First-In First-Out Memory System With Shift Register Fill Indication

ABSTRACT OF THE DISCLOSURE

[0047] An electronic device (10). The device comprises a memory structure (12) comprising an integer M of word storage locations. The device further comprises a write shift register (SR_{WT}) for storing a sequence of bits. The sequence in the write shift register comprises a number of bits equal to a ratio of $1/R_1$ times the integer M. The device further comprises circuitry (16) for providing a write clock cycle to the write shift register for selected write operations with respect to any of the word storage locations. In response to each write clock cycle, received from the circuitry for providing the write clock cycle, the write shift register shifts the sequence in the write shift register. Further, one bit in the sequence in the write shift register corresponds to an indication of one of the memory word storage locations into which a word will be written. The device further comprises a read shift register (SR_{RD}) for storing a sequence of bits. The sequence in the read shift register comprises a number of bits equal to a ratio of $1/R_2$ times the integer M. The device further comprises circuitry (16) for providing a read clock cycle to the read shift register for selected read operations with respect to any of the word storage locations. In response to each read clock cycle, received from the circuitry for providing the read clock cycle, the read shift register shifts the sequence in the read shift register. Further, one bit in the sequence in the read shift register corresponds to an indication of one of the memory word storage locations from which a word will be read. Lastly, the device comprises circuitry (18_x) for evaluating selected bits in the sequence in the write register relative to selected bits in the sequence in the read register for detecting a level of data fullness in the memory structure.